REMARKS

Claims 1-3 and 9 remain in the present application. Previously added claim 8 has been renumbered as claim 9 in this response. No new matter has been introduced as a result of the amendment. Favorable reconsideration is respectfully requested.

Claim 1 was rejected under 35 U.S.C. §102(a) as being unpatentable over *Nelson et al.* (U.S. Patent No. 5,812,857). Claims 1-3 were also rejected under 35 U.S.C. §103(a) as being unpatentable over *Li et al.* (U.S. Patent No. 6,012,088) in view of *Tang et al.* (U.S. Patent No. 6,298,370). Applicants traverse these rejections. Favorable reconsideration is respectfully requested.

Nelson does not teach or suggest the feature of "automatically reconfiguring the FPGA hardware structure of the computer with the aid of the hardware portion of the first configuration data so that the computer exhibits a hardware structure configured to the first task; and processing the first task with the computer configured with the first configuration data" as recited in claims 1 and similarly recited in claim 9.

As was argued previously by Applicant, *Nelson* does not disclose a Field Programmable Gate Array (FPGA) configuration. FPGA's are known in the art as semiconductor devices used to process digital information, utilizing gate array technology that can be reprogrammed as hardware after it is manufactured, rather than having its programming fixed during the manufacturing. In contrast, *Nelson* discloses that the field configurable embedded computer system contains a central processing unit, a persistent memory area for storing programs and persistent variables that need to be preserved when the product is powered down, a volatile memory area that is operational while the unit containing the field configurable embedded computer system is powered on, but is erased when the unit is powered off, and a network communications hardware means, including the associated software drivers that enable the device to connect to a computer network (col. 1, lines 17-27; col. 4, lines 12-25). The persistent memory is disclosed as a conventional flash memory (i.e., EEPROM), and the volatile memory is disclosed as RAM (col. 4, lines 15-22; col. 5, lines 1-27; see claim 2). In other words, the teaching in *Nelson* illustrates the use of a field programmable *computer system within a network* using a conventional topology, while the present claims explicitly require the use of FPGA's.

Nelson specifically teaches an apparatus and method for downloading firmware upgrades to a targeted remote field configurable embedded computer system over a computer network (see Abstract). As is commonly known in the art, "firmware" refers to software that is embedded in a hardware device that is used as a functional replacement for hardware on low cost microprocessors. Regarding the Office Action's Response on pages 5-6, this rationale is simply incorrect – loading new driver software into RAM memory in no way teaches reconfiguraing a hardware structure of the computer with the aid of the hardware portion of the first configuration data. Again, as is generally known in the art, a device driver (or, "driver" for short), is a computer program that enables another program, typically an operating system (OS), to interact with a hardware device. Thus the loaded network driver of Nelson (col. 5, lines 19-29) reconfigures the software structure of the computer, but nothing whatsoever is disclosed in Nelson that teaches the reconfiguration of any hardware structure. In fact, Nelson explicitly teaches that the "field configurable embedded computer system" must not contain any changes to the hardware structure:

> Field configurable embedded computer systems are used to build a family of products. Each product in the family uses the same field configurable computer system hardware. The family members differ from each other in the feature functions they provide. The feature functions for a particular family member are implemented in computer software. Thus by changing the software, a product can be changed from one family member to another.

(col. 1, lines 29-36) (emphasis added). For at least this reason, Applicants submit the rejection is improper.

Furthermore, the present claims recite that the FPGA hardware structure of the computer is reconfigured with the aid of the hardware portion of the first configuration data (see application specification page 2). This limitation is not taught in *Nelson*. As was provided in the above arguments, *Nelson* teaches a set of network driver codes which are downloaded from a master computer to a configurable embedded computer system within a network. The main feature disclosed in *Nelson* is that the network drivers and the feature functions are combined to eliminate redundant drivers, and also eliminate independent download program code sections (col. 4, lines 41-62). *Nelson* teaches that the feature functions are simply programmable code (col. 5, lines 29-37; see claims 1 and 3 – "feature functions, including a download program code

section that contains a download program"). Accordingly, *Nelson* teaches that the drivers are accompanied by their associated software used in operation.

Applicants would like to note that there is no equivalence

Addressing the Office Action's remarks in paragraphs 8, 9, 12 and 13, the passages cited support the Applicant's arguments stated above – namely, that *Nelson* only teaches the upgrade of software, via drivers and programmable code (col. 1, lines 10-13). *Nelson* is completely silent with regard to FPGA's as well as the assistance of a hardware portion of configuration data in reconfiguring the hardware structure. Applicants further request that the Examiner kindly point out what distinctions are being made between "software" and "hardware" portions in Nelson. As the interpretation of the teachings in Nelson are clearly exceeding beyond the scope of the disclosure contained therein. Applicants respectfully submit that the rejection under 35 U.S.C. §102 is improper and should be withdrawn.

Regarding *Li,* the reference also fails to teach or suggest "automatically reconfiguring the FPGA hardware structure of the computer with the aid of the hardware portion of the first configuration data so that the computer exhibits a hardware structure configured to the first task; and processing the first task with the computer configured with the first configuration data" as recited in claim 1. Applicants maintain that no FPGA structure whatsoever is disclosed in the reference. Furthermore Li fails to teach where a hardware portion of the configuration data is disclosed anywhere in the document. The Examiner's Response (paragraphs 10-11) fails to address any of the Applicant's concerns highlighted in previous office actions. *Li* merely discloses an Internet access device (col. 7, lines 13-19) which is able to automatically configure software for communications with the Internet using information contained in a configuration record. *Li* teaches that, before the Internet access device configures itself, the customer and an Internet service provider communicate in order to determine an appropriate level of service for that customer and corresponding configuration information for the Internet access device. Once the customer has specified his needs, the ISP assembles all of this customer information and inputs it into an ISP database. Some of this customer information comes from the customer itself (e.g., a desired domain name), while some information is generated by the ISP itself (e.g., the IP address block). Using the information in this database, the ISP is then able to generate a configuration file for future use by the customer. The configuration file contains all of the

configuration needed by the customer to configure his Internet access device for the customer's desired level of service (col. 9, lines 25-62). In terms of hardware, the only teaching provided by *Li* is that the configuration record may be modified by the user or the ISP if the user physically changes the hardware within the computer and prearranges the change with the ISP (i.e., switches from a modem to an ISDN line; col. 15, lines 16-54). Nothing in the disclosure of *Li* teaches the features recited above.

Similarly, *Tang* does not solve the deficiencies of *Li* discussed above, and furthermore it is respectfully submitted that improper hindsight was used to combine these references. The disclosure in *Tang* deals with operating a computer system having a stored operating system and application program with a first processor having an instruction set, and a second processor having a different instruction set to address problem in "CPU-centric" systems where the selection of the CPU determines the system's processing capabilities and add-in-cards are added to the CPU to add specific applications or functions, such as modem or multimedia. (col. 3, lines 35-40). There is no conceivable teaching, suggestion or motivation for one having ordinary skill in the art to combine the references in the manner suggested in the Office Action. The "configuration data" of *Tang* is wholly unrelated to that of *Li*. As such it is also respectfully submitted that the rejection under 35 U.S.C. §103 is also improper and should be withdrawn.

In light of the above, Applicants respectfully submit that independent claims 1 and 9 of the present application as well as dependant claims 2-3 are both novel and non-obvious over the art of record. Accordingly, Applicants respectfully request that a timely Notice of Allowance be issued in this case. If any additional fees are due in connection with this application as a whole, the Examiner is authorized to deduct said fees from Deposit Account No.: 02-1818. If such a deduction is made, please indicate the attorney docket number (0114543-002) on the account statement.

Respectfully submitted,

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